REMARKS

Claims 1-23 were pending in this application.

Claims 1-23 have been rejected.

Claim 17 has been amended as shown above.

Claims 1-23 remain pending in this application.

Reconsideration and full allowance of Claims 1-23 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-23 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,856,975 to Rostoker et al. ("*Rostoker*"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Office Action asserts that column 9, lines 31-40 and column 28, lines 55-65 of *Rostoker* anticipate a "read only memory" that stores an "embedded control program," which is executed by a microcontroller to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17. (*Office Action, Page 1, Fifth paragraph*).

The first cited portion of *Rostoker* (column 9, lines 31-40) recites a "physical layer

interface circuit" (element 332) and a "network protocol processing unit" (element 333). (*Col. 9, Lines 31-34*). The network protocol processing unit is connected to a programmable ROM (PROM). (*Col. 9, Lines 39-41*). This portion of *Rostoker* simply mentions that a network protocol processing unit is coupled to a physical layer interface circuit and a programmable ROM. The first cited portion of *Rostoker* fails to mention that the PROM includes an "embedded control program." More specifically, this portion of *Rostoker* fails to mention that the PROM stores a program used to control the physical layer interface circuit. As a result, this portion of *Rostoker* fails to anticipate a "read only memory" storing an "embedded control program" executed by a microcontroller to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17.

The second cited portion of *Rostoker* (column 28, lines 55-65) recites that an "address sourcing capability" of "the DMA" can be "used to boot from a ROM or some other device." (*Col. 28, Lines 59-61*). This portion of *Rostoker* also fails to mention that the ROM stores a program used to control a physical layer interface. As a result, this portion of *Rostoker* also fails to anticipate a "read only memory" storing an "embedded control program" executed by a microcontroller to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17.

The Office Action also asserts that column 5, lines 1-5 of *Rostoker* anticipate a "random access memory" that stores a "software control program," which is executed by a microcontroller to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17. (*Office Action, Page 1, Sixth paragraph*).

Rostoker recites that a high speed digital video network apparatus includes "network protocol processing system interconnection circuits" and "compression/decompression

encoder/decoder circuits." (*Col. 4, Lines 29-33*). The interconnection circuits include a "Physical-layer medium dependent (PMD) circuit," a "virtual channel memory," a "direct memory access (DMA) controller," and a RISC microprocessor. (*Col. 4, Lines 34-60*). The DMA controller is responsible for connecting the virtual channel memory and the compression/decompression circuits. (*Col. 4, Lines 47-50*). The RISC microprocessor is responsible for controlling the DMA controller and for controlling transfers involving the virtual channel memory. (*Col. 4, Lines 54-56*).

The cited portion of *Rostoker* (column 5, lines 1-5) recites that a program for the RISC microprocessor is stored as firmware in a RAM, where the firmware can be downloaded. (*Col. 5, Lines 1-5*). This portion of *Rostoker* simply recites the use of a RAM. This portion of *Rostoker* fails to mention that the RAM stores a program used to control a physical layer interface. In particular, this portion of *Rostoker* clearly recites that the RISC microprocessor controls the DMA controller and transfers involving the virtual channel memory, not the "Physical-layer medium dependent (PMD) circuit." As a result, this portion of *Rostoker* fails to anticipate a "random access memory" storing a "software control program" executed by a microcontroller to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17.

In addition, the Office Action asserts that column 4, lines 34-60 and column 5, lines 1-5 of *Rostoker* anticipate a "microcontroller" that executes an "embedded control program" or a "software control program" depending on an operating mode, where both programs are used to "control [a] physical layer interface" as recited in Claims 1, 9, and 17. (*Office Action, Page 1, Last paragraph*).

The first cited portion of *Rostoker* (column 4, lines 34-60) mentions the use of a DMA

controller and a RISC microprocessor. However, this portion of *Rostoker* does not recite any structure for controlling the "Physical-layer medium dependent (PMD) circuit." Instead, as described above, the DMA controller is responsible for connecting the virtual channel memory and the compression/decompression circuits, and the RISC microprocessor is responsible for controlling the DMA controller and transfers involving the virtual channel memory. Neither the DMA controller nor the RISC microprocessor is described in this portion of *Rostoker* as controlling a physical layer interface. As a result, this portion of *Rostoker* fails to anticipate a "microcontroller" that executes an "embedded control program" or a "software control program" to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17.

As described above, the second cited portion of *Rostoker* (column 5, lines 1-5) recites that a program for the RISC microprocessor is stored in a RAM. This portion of *Rostoker* simply recites that the RISC microprocessor (which only controls the DMA controller and transfers involving the virtual channel memory) has access to instructions in a RAM. The second cited portion of *Rostoker* contains absolutely no mention that the program stored in the RAM is used to control a physical layer interface. As a result, this portion of *Rostoker* also fails to anticipate a "microcontroller" that executes an "embedded control program" or a "downloadable software control program" to "thereby control [a] physical layer interface" as recited in Claims 1, 9, and 17.

For these reasons, the Office Action has failed to establish that *Rostoker* anticipates the Applicants' invention as recited in Claims 1, 9, and 17 (and their dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1-23.

II. CONCLUSION

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request an early allowance of such claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned attorney at the telephone number indicated below or at *wmunck@davismunck.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to the Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: May 24, 2004

William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *wmunck@davismunck.com*